3N90

900V N-Plance Enhancement Mode MOSFET

Description

The 3N90 is silicon N-channel Enhanced

VDMOSFETs, is obtained by the self-aligned planar Technology

which reduce the conduction loss, improve switching

performance and enhance the avalanche energy. The transistor

can be used in various power switching circuit for system

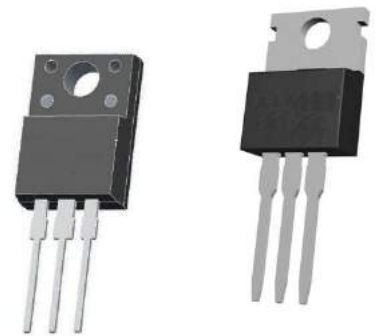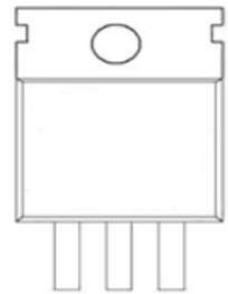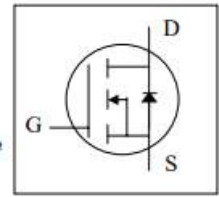miniaturization and higher efficiency.

General Features

VDS =900V,ID =3A

RDS(ON) <4.8Ω@ VGS=10V

Application

Uninterruptible Power Supply(UPS)

Power Factor Correction (PFC)

Absolute Maximum Ratings (T$_C$=25℃ unless otherwise noted)

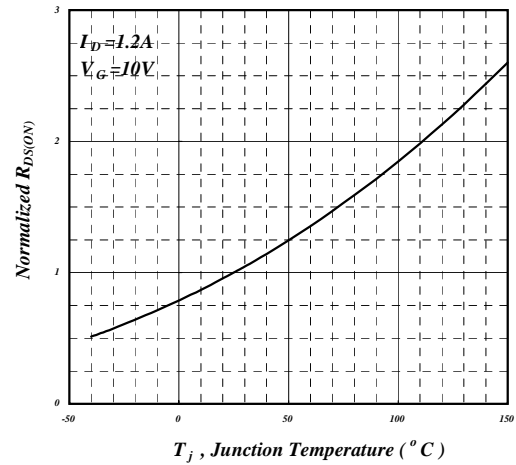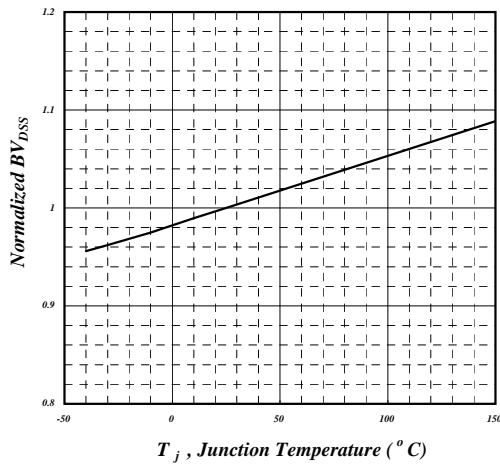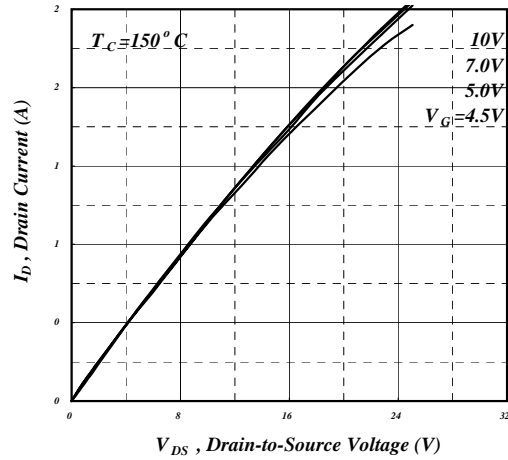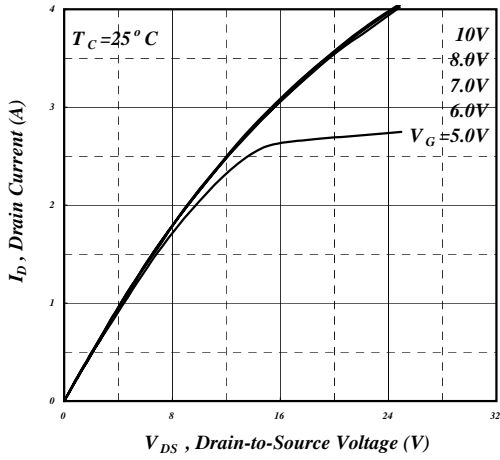| Symbol	Parameter	Rating	Units
VDS	Drain-Source Voltage	900	V
VGS	Gate-Source Voltage	+30	V
I$_D$@T$_C$=25℃	Drain Current, V$_{GS}$ @ 10V[4]	3	A
I$_D$@T$_C$=100℃	Drain Current, V$_{GS}$ @ 10V[4]	1.89	A
IDM	Pulsed Drain Current[1]	10	A
P$_D$@T$_C$=25℃	Total Power Dissipation	25	W
EAS	Single Pulse Avalanche Energy[3]	4.5	mJ
IAR	Avalanche Current	3	A
TSTG	Storage Temperature Range	-55 to 150	℃
T$_J$	Operating Junction Temperature Range	-55 to 150	℃
Rthj-c	Maximum Thermal Resistance, Junction-case	5	℃/W
Rthj-a	Maximum Thermal Resistance, Junction-ambient	65	℃/W

900V N-Plance Enhancement Mode MOSFET

Electrical Characteristics@T_j=25ºC(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250uA	900	-	-	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance[2]	V_{GS}=10V, I_D=1.2A	-	-	4.8	Ω
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250uA	2	-	4	V
g_{fs}	Forward Transconductance	V_{DS}=10V, I_D=1A	-	2	-	S
I_{DSS}	Drain-Source Leakage Current	V_{DS}=720V, V_{GS}=0V	-	-	25	uA
I_{GSS}	Gate-Source Leakage	V_{GS}=±30V, V_{DS}=0V	-	-	±100	nA
Q_g	Total Gate Charge[2]	I_D=1A	-	18	29	nC
Q_{gs}	Gate-Source Charge	V_{DS}=540V	-	3.5	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge	V_{GS}=10V	-	7	-	nC
$t_{d(on)}$	Turn-on Delay Time[2]	V_{DD}=300V	-	20	-	ns
t_r	Rise Time	I_D=1A	-	14	-	ns
$t_{d(off)}$	Turn-off Delay Time	R_G=50Ω	-	105	-	ns
t_f	Fall Time	V_{GS}=10V	-	24	-	ns
C_{iss}	Input Capacitance	V_{GS}=0V	-	800	1280	pF
C_{oss}	Output Capacitance	V_{DS}=25V f=1.0MHz	-	55	-	pF
C_{rss}	Reverse Transfer Capacitance		-	4	-	pF
R_g	Gate Resistance	f=1.0MHz	-	4	6	Ω
V_{SD}	Forward On Voltage[2]	I_S=1.2A, V_{GS}=0V	-	-	1.5	V
t_{rr}	Reverse Recovery Time[2]	I_S=1A, V_{GS}=0V dI/dt=100A/µs	-	320	-	ns
Q_{rr}	Reverse Recovery Charge		-	1.3	-	µC

Notes:

1.Pulse width limited by max. junction temperature.

2.Pulse test

3.Starting T_j=25ºC , V_{DD}=50V , L=1mH , R_G=25Ω

4.Ensure that the junction temperature does not exceed $T_{Jmax.}$.

Fig 4. Normalized On-Resistance
v.s. Junction Temperature

DSS v.s. Junction
Temperature
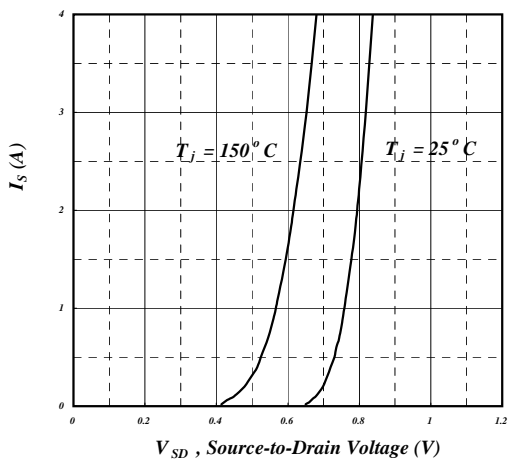

g 5. Forward Characteristic of
Reverse Diode
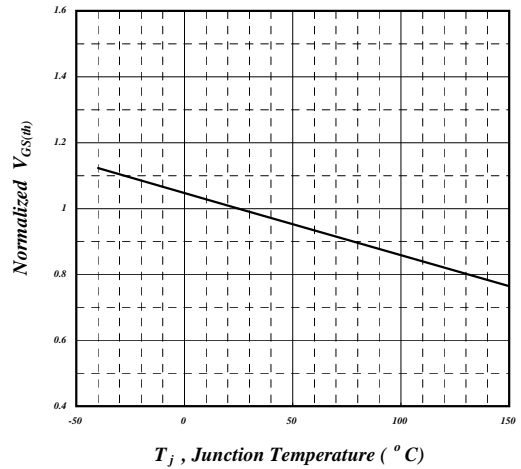
Fig 6. Gate Threshold Voltage v.s.
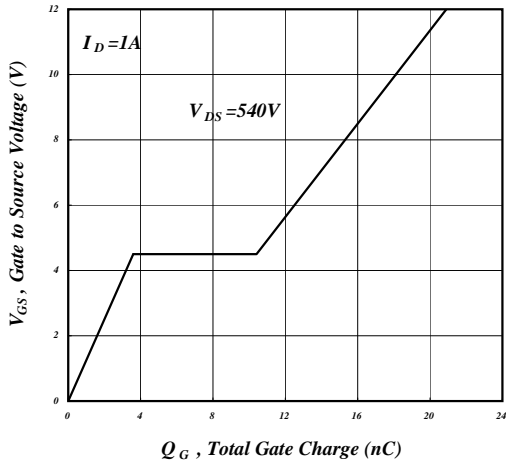Junction Temperature
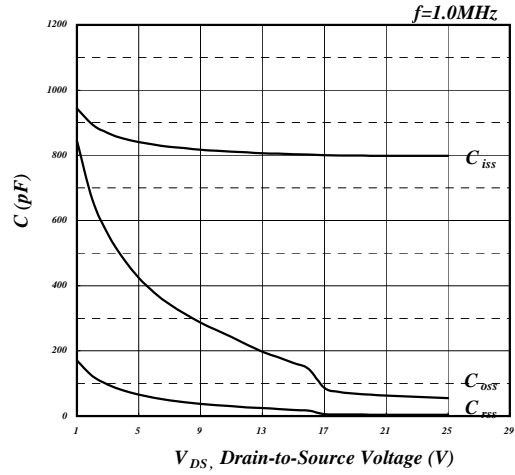
Fig 7. Gate Charge Characteristics
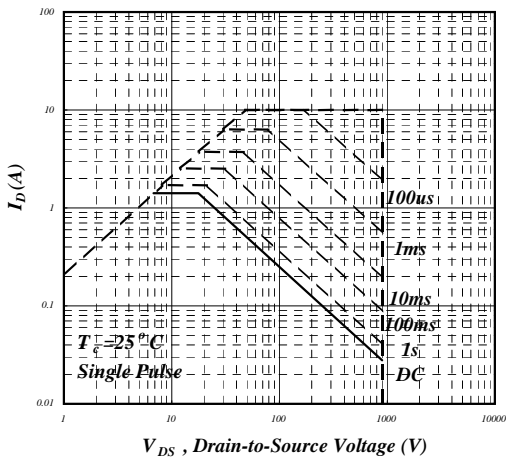

Fig 8. Typical Capacitance Characteristics
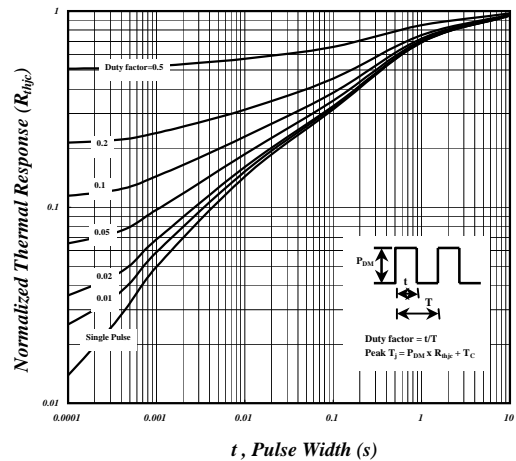

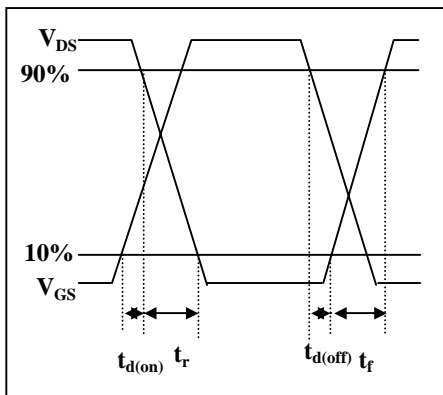Fig 9. Maximum Safe Operating Area

Fig 10. Effective Transient Thermal Impedance
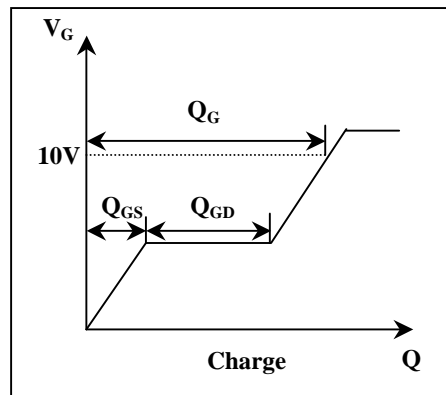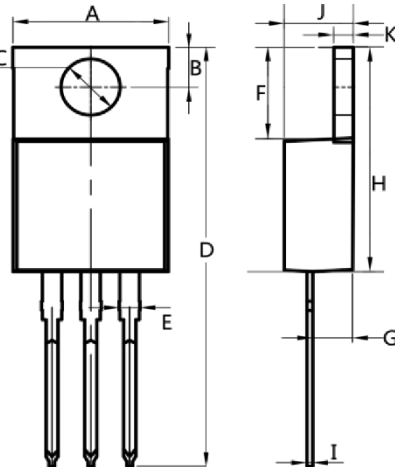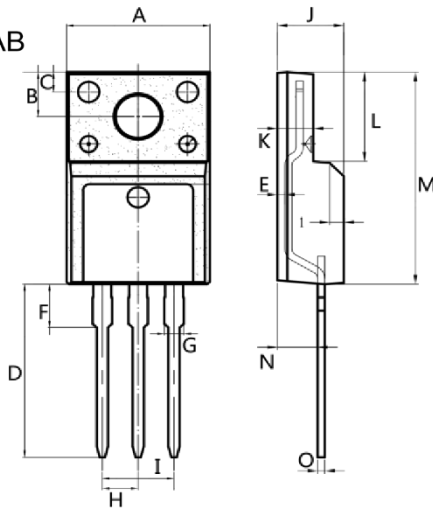

Fig 11. Switching Time Waveform

Fig 12. Gate Charge Waveform

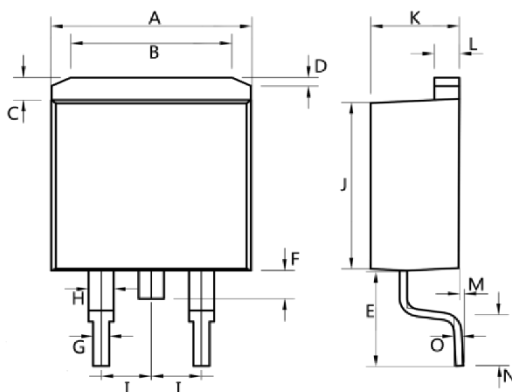## 900V N-Plance Enhancement Mode MOSFET

TO-220AB

Dim.	Min.	Max.
A	10.0	10.4
B	2.5	3.0
C	3.5	4.0
D	28.0	30.0
E	1.1	1.5
F	6.2	6.6
G	2.9	3.3
H	15.0	16.0
I	0.35	0.45
J	4.3	4.7
K	1.2	1.4
All Dimensions in millimeter		

ITO-220AB

Dim.	Min.	Max.
A	9.9	10.3
B	2.9	3.5
C	1.15	1.45
D	12.75	13.25
E	0.55	0.75
F	3.1	3.5
G	1.25	1.45
H	Typ	2.54
I	Typ	5.08
J	4.55	4.75
K	2.4	2.7
L	6.35	6.75
M	15.0	16.0
N	2.75	3.15
O	0.45	0.60
All Dimensions in millimeter		

TO-263

Dim.	Min.	Max.
A	10.0	10. 5
B	7.25	7.75
C	1.3	1.5
D	0.55	0.75
E	5.0	6.0
F	1.4	1.6
G	0.75	0.95
H	1.15	1.35
I	Typ	2.54
J	8.4	8.6
K	4.4	4.6
L	1.25	1.45
M	0.02	0.1
N	2.4	2.8
O	0.35	0.45
All Dimensions in millimeter		